UNITED STATES PATENT AND TRADEMARK OFFICE

NV

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,146	10/21/2003	Austin H. Lesea	X-1383 US	6602

24309 7590 01/14/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,146	LESEA, AUSTIN H.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11,12 and 14-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,12,14-17,21 and 26* is/are rejected.

7)☒ Claim(s) *18-20 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 16 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of "*wherein the sum of the delays is less than the period of the input clock signal*" is not described in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-8,11, 12, 14-17, 21 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Lacey (U. S. PAT. 6,651,181).

In claims 1 and 4 Lacey teaches all claimed features in Figs. 1-3, a semiconductor device comprising: a clock input terminal (114) for receiving an input clock signal; a digital clock manager (100), comprising a plurality of series connected delay elements (inside 144) coupled to a multiplexer (146), for generating a plurality of

clock signals (GCLK3:0) in response to the input clock signal, wherein the plurality of clock signals are delayed versions of the input clock signal; a plurality of input/output blocks (110a-110n), including a first set of IOBs (110a, 110h) configured to operate in response to a first clock signal (GCLK0) of the plurality of clock signals, a second set of IOBs (110b, 110f,110g, 110i) configured to operate in response to a second clock signal (GCLK1) of the plurality of clock signals, and a third set of IOBs (110c, 110n) configured to operate in response to a third clock signal (GCLK2) of the plurality of clock signals; wherein the first, second and third sets of IOBS are interleaved along a perimeter of the semiconductor device,

In claim 2, Lacey further teaches, the semiconductor device of Claim 1 in col. 6, lines 45-53, wherein the first clock signal (GCLK0) is synchronous with the input clock signal, the second clock signal is delayed by a phase angle of 90 degrees with respect to the first clock signal, and the third clock signal is delayed by a phase angle of 180 degrees with respect to the first clock signal (col. 6, lines 45-53).

In claim 3, Lacey further teaches, the semiconductor device of Claim 1 in col. 6, lines 45-53, wherein each of the plurality of clock signals is delayed by a predetermined phase (90 degrees) with respect to the input clock signal.

In claim 5, Lacey further teaches, the semiconductor device of Claim 1, wherein the plurality of input/output blocks further includes a fourth set of IOBs (110d, 110e) configured to operate in response to a fourth clock signal of the plurality of clock signals.

In claim 6, Lacey further teaches, the semiconductor device of Claim 1, wherein each of the plurality of clock signals has the same wherein each of the frequency (inherent).

In claim 7, Lacey further teaches the semiconductor device of Claim 1, wherein each of the plurality of clock signals exhibits a rising edge during a single period of the input clock signal (inherent).

Method claims 8, 11, 12, 14 and 15 correspond to detailed circuitry already discussed similarly with regard to claims 1-7.

In claim 16, Lacey teaches all claimed features in Figs. 1-3, a method of operating a semiconductor device comprising: determining a period (half cycle) of an input clock signal (INCLK0); introducing a plurality of discrete delays (144 inherently comprising delays such as inverters) to the input clock signal, thereby generating a corresponding plurality of delayed clock signals (GCLK3:0); and using the plurality of delayed clock signals to control output switching of the semiconductor device (intended use recitation).

In claim 17, Lacey further teaches the semiconductor device of Claim 16, wherein the step of determining the period of the input clock signal comprises: applying the input clock signal to a delay line having a plurality of series-connected delay elements (144 inherently comprising delays such as inverters); and selecting an output clock signal (GCLK0) from the delay line such that the output clock signal is synchronized with the input clock signal.

In claim 21, Lacey teaches all claimed features in Figs. 1-3, a semiconductor device comprising: a digital clock manager (128) configured to identify a period of an input clock signal (INCLK3:0); a plurality of series-connected programmable delay lines (144 inherently comprising programmable delay lines) configured to provide a corresponding plurality of delayed clock signals (CLK0-CLK315) in response to the input clock signal; and delay control circuitry (130) coupled to the digital clock manager and the programmable delay lines, wherein the delay control circuitry (130) is configured to program a delay in each of the plurality of series-connected programmable delay lines in response to the period of the input clock signal.

Claim 26 corresponds to detailed circuitry already discussed similarly with regard to claim 16.

4. Claims 18-20 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***

VIBOL TAN
PRIMARY EXAMINER